PROCESSOR HAVING A COMPARE EXTENSION OF AN INSTRUCTION SET ARCHITECTURE

ABSTRACT OF THE INVENTION

A processor having a compare extension of an instruction set architecture which incorporates a set of high performance floating point operations. The instruction set architecture incorporates a variety of data formats including single precision and double precision data formats, as well as the paired-single data format that allows two simultaneous operations on a pair of operands. The extension includes instructions directed to a magnitude compare of floating point numbers and conversions between a pair of 32-bit fixed point integers and paired-single floating point format.